IN THE CLAIMS:

Please amend the claims as follows. The claims are in the format as required by 35 C.F.R. § 1.121.

1. (Currently Amended) A method for reducing CPU code latency by writing data to hardware devices on behalf of said CPU, the method comprising:

directing logic associated with a register to drive data ~~via~~ to a first device;

driving the data ~~via~~ from the register to the first device and a second device simultaneously;

sampling ~~of~~ the data ~~by the register~~ and determining whether the data is valid, wherein the data is sampled and validity is determined by logic associated with the register; and

signaling the second device as to whether the data is valid or invalid.

2. (Currently Amended) The method for reducing CPU code latency by writing data to hardware devices on behalf of said CPU according to claim 1, wherein the logic associated with the register is capable of analyzing at least one bit of the data to determine if the data is valid or invalid.

3. (Original) The method for reducing CPU code latency by writing data to hardware devices on behalf of said CPU according to claim 2, wherein the bit analyzed in determining the validity of the data is at least one of a most significant bit and a least significant bit.

4. (Original) The method for reducing CPU code latency by writing data to hardware devices on behalf of said CPU according to claim 2, wherein the first device comprises a CPU.

5. (Original) The method for reducing CPU code latency by writing data to hardware devices on behalf of said CPU according to claim 1, wherein the second device comprises a memory device.

6. (Original) The method for reducing CPU code latency by writing data to hardware devices on behalf of said CPU according to claim 5, wherein the memory device further comprising at least one of a content addressable memory, a hardware register and a storage medium.

7. (Original) An apparatus for reducing CPU bus cycle time and CPU latency in responding to real-time events, the apparatus comprising:

a CPU in communication with and capable of directing a first hardware device;

the first hardware device responsive to the CPU and capable of driving data pursuant to instructions from the CPU, wherein the hardware device is further capable of:

substantially simultaneously driving data to the CPU and a second hardware device;

analyzing one or more bits from the data driven by the first hardware device in determining validity of the data; and

transmitting a signal to the second hardware device regarding the validity of the data.

8. (Currently Amended) The apparatus for reducing CPU bus cycle time and CPU latency in responding to real-time events according to claim 7, wherein the first hardware device comprises a hardware register and associated logic.

9. (Original) The apparatus for reducing CPU bus cycle time and CPU latency in responding to real-time events according to claim 8, wherein the second hardware device comprises a writable hardware device.

10. (Currently Amended) The apparatus for reducing CPU bus cycle time and CPU latency in responding to real-time events according to claim 9, wherein the writable hardware device comprises at least on one of a storage medium, content address memory and a register.

11. (Currently Amended) The apparatus for reducing CPU bus cycle time and CPU latency in responding to real-time events according to claim 7, wherein the first hardware device analyzes

at least one of a most-significant-bit and a least significant bit in determining the validity of the data.

12. (Original) The apparatus for reducing CPU bus cycle time and CPU latency in responding to real-time events according to claim 7, wherein the validity signal is transmitted to the second hardware device at approximately near completion of a read cycle of the CPU.

13. (Currently Amended) An apparatus for reducing CPU latency by reducing CPU bus read/write cycles, the apparatus comprising:

a hardware device ~~register~~ capable of testing data for one or more validity bits, wherein the hardware device further comprises a register and associated logic;

a CPU in communication with the hardware ~~register~~ device during a first bus cycle, wherein the CPU directs the hardware ~~register~~ device to drive the data substantially simultaneously to the CPU and a second register and in close proximity to the data transfer, the hardware ~~register~~ device sends a validity signal to the second register without a subsequent bus cycle instruction to the second register from the CPU.